

**LISTING OF CLAIMS**

1-10. (Canceled)

11. (Original) A semiconductor wafer comprising:

at least one active area;

at least one resistor having a resistive region obtained within said active area; and

a delimitation structure set on top of said active area to delimit said resistive region.

12. (Original) The wafer according to claim 11, wherein said delimitation structure is made of a material used in the semiconductor industry.

13. (Original) The wafer according to claim 12, wherein said delimitation structure is made of a material selected from a group consisting of a dielectric, a semiconductor and a metal.

14. (Original) The wafer according to claim 12, wherein said delimitation structure is made of polysilicon.

15. (Currently Amended) The wafer according to claim 11, further characterized by comprising protective elements which extend within said delimitation structure and coat said resistive region.

16. (Original) The wafer according to claim 15, wherein said protective elements are made of a dielectric material.

17. (Original) An integrated device comprising:  
a semiconductor body;  
at least one active area on the semiconductor body;  
at least one resistor having a resistive region within said active area;  
a delimitation structure set on top of said active area to delimit said resistive region.

18. (Original) The integrated device according to claim 17, wherein said delimitation structure is made of a material used in the semiconductor industry.

19. (Original) The integrated device according to claim 18, wherein said delimitation structure is made of a material selected from a group consisting of a dielectric, a semiconductor and a metal.

20. (Original) The integrated device according to claim 18, wherein said delimitation structure is made of polysilicon.

21. (Currently Amended) The integrated device according claim 17, further ~~characterized by~~ comprising protective elements which extend within said delimitation structure and coat said resistive region.

22. (Original) The integrated device according to claim 21, wherein said protective elements are made of a dielectric material.

23-31. (Canceled)

32. (New) An integrated circuit, comprising:  
a substrate including an active region;  
a resistor formed within the active region of the substrate;  
a delimiter structure formed over the substrate and defining a mask used for ion implantation to form the resistor; and  
a spacer extending between the delimiter structure to cover the resistor formed in the active region but not cover a top surface of the delimiter structure;  
wherein the delimiter structure is silicided to form contacts with the resistor.

33. (New) An integrated resistive element having protection from silicidation, comprising:  
at least one active area in a semiconductor substrate;  
at least one resistive region having a pre-set resistivity in said active area;  
a delimitation structure that delimits said resistive region on top of said active area; and  
a salicidation protective structure which extends within said delimitation structure and covers said resistive region.

34. (New) The element according to claim 33, wherein said salicidation protective structure is made of a material selected from the group consisting of: silicon dioxide, silicon nitride, and silicon oxynitride.

35. (New) The element according to claim 33, wherein said delimitation structure is made of polysilicon.

36. (New) An integrated circuit, comprising:  
an active area defined in a semiconductor substrate;  
a resistive region having a pre-set resistivity formed in the active area;  
a polysilicon structure which delimits the resistive region; and  
a protective layer over the resistive region between the polysilicon structure;  
wherein the polysilicon structure is silicided without affecting the pre-set resistivity in the active area.

37. (New) The circuit according to claim 36, wherein the protective layer is made of a material selected from the group consisting of: silicon dioxide, silicon nitride, and silicon oxynitride.